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EXAMINER	
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ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/580,625	HUETING ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/10/2009 has been entered.

Claim Objections

2. **Claims 1-18 and 20** are objected to because of the following informalities:

3. Claim 1 recites the limitation 'the doping concentration" in the 4th last line of the claim and it is suggested to change this limitation to "a doping concentration".

4. Claim 1 recites the limitation 'the part of the drift region adjacent to the body" in the 4th and 3rd last lines of the claim and it is suggested to change this limitation to "a part of the drift region adjacent to the body".

5. Claim 1 recites the limitation 'the part of the drift region adjacent to the drain region" in the 3rd and 2nd last lines of the claim and it is suggested to change this limitation to "a part of the drift region adjacent to the drain region".

6. Claim 3 recites the limitation 'the gap" in the 2nd last line of the claim and it is suggested to change this limitation to "a gap".

7. Claim 3 recites the limitation 'the sidewalls" in the 2nd and 3rd last lines of the claim and it is suggested to change this limitation to "sidewalls".

8. Claim 8 recites the limitation 'the doping" in the 2nd last line of the claim and it is suggested to change this limitation to "a doping concentration".

9. Claim 9 recites the limitations 'the thickness" in the 2nd last and the last lines of the claim and it is suggested to change these limitations to "a thickness".

10. Claim 15 recites the limitation 'the part of the drift region adjacent to the body region" in the 4th last line of the claim and it is suggested to change this limitation to "a part of the drift region adjacent to the body region".

11. Claim 15 recites the limitation 'the part of the drift region adjacent to the drain region" in the 4th and 3rd last lines of the claim and it is suggested to change this limitation to "a part of the drift region adjacent to the drain region".

12. Claim 20 recites the limitation 'the gap" in the 2nd last line of the claim and it is suggested to change this limitation to "a gap".

13. Claim 20 recites the limitation 'the sidewalls" in the 4th last line of the claim and it is suggested to change this limitation to "sidewalls".

14. Claims 2, 4-7, 10-14, and 16-18 are rejected because they depend on the rejected claims 1 and 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. **Claims 15-18** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 15 recites "the doping concentration in the part of the drift region adjacent to the drain region being at least an order of magnitude greater than the doping concentration in the part of the drift region adjacent to the body region", which has a scope not fully support by the original disclosure. The specification indicates that the doping concentration in the drift region is such that the doping concentration adjacent to the drift region is higher than the doping concentration adjacent to the body region by a factor of at least 50 [page 3 lines 6-10], at least 100 [page 3 lines 14-19], at least 200 [page 3 lines 14-19], 100 [page 9 lines 12-18; page 10 lines 1-6], or 200 [page 7 lines 21-26]. The limitation "at least an order of magnitude greater than" does not have the full support from the original disclosure because it has a scope broader than the scopes in the original disclosure. Claims 16-18 are rejected because they depend on the rejected claim 15.

17. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

18. **Claims 5-6 and 10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

19. Claim 5 recites the limitation "the surface" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 10 recites the limitation "the cell pitch" in the first two lines of the claim. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 6 is rejected because it depends on the rejected claim 5.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. **Claims 1, 4-7, 9-10, and 12-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (EP 1168455 A2) as can be understood since claims 5-6, 10, and 15-18 have been rejected under 35 U.S.C. 112.

25. Regarding **claim 1**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate

insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and the doping concentration in the drift region (12) increases from the part of the drift region (12) adjacent to the body region (13) to the part of the drift region (12) adjacent to the drain region (11; see Fig. 15B, paragraph [0053]),

Omura et al. do not teach the gate-field plate insulator (18) being at least as thick as the field plate insulator (16), and the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

26. Regarding **claim 4**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.

Omura et al. teach a device with a breakdown voltage of 50V (paragraph [0045]). Omura et al. also teach that the breakdown voltage and the ON resistance satisfy the inequality: Ron < $2.2 \times 10^{-5} Vb^{2.25}$.

Parameters such as the breakdown voltage and the ON resistance in the art of semiconductor manufacturing process are the tradeoff between the device's performance and reliability and are subject to changes due to the requirement of the application, e.g. whether the performance (lower ON resistance) is more important than the reliability (higher break down voltage). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to lower the breakdown voltage to less than or equal to 30V as claimed in order to achieve a lower ON resistance to improve device performance.

27. Regarding **claim 5**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions (14) and the insulated trenches (15) arranged across the first major surface (the top surface of 13) is a pattern in which cells repeat in more than one direction across the surface to form a three-dimensional cell structure (see Fig. 25).

28. Regarding **claim 6**, Omura et al. also teach an insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern (see Fig. 25)

29. Regarding **claim 7**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]) extending through the

source region (14) to the body region (13) to connect a source contact (source electrode 21) to the source region (14) and the body region (13; see Fig. 4).

30. Regarding **claim 9**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the thickness of the insulator (16; Fig. 2) adjacent to the conductive field plate electrode (17) is greater than the thickness of the insulator (18) adjacent to the conductive gate electrode (19; see Fig. 2, paragraph [0031]).

31. Regarding **claim 10**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the cell pitch is not greater than 1 micron.

Parameters such as the cell pitch in the art of semiconductor manufacturing process are subject to change due to the requirement of the device performance. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use a cell pitch not greater than 1 micron as claimed to achieve the required performance.

32. Regarding **claim 12**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the field plate insulator (16) has a thickness between 0.6 to 1 microns and the gate insulator (18) has a thickness between 0.2 to 0.5 microns.

Omura et al. teach that the thickness of the field plate oxide (16) is determined by the breakdown voltage and the thickness of the gate oxide (18) is determined by the threshold voltage (paragraph [0031]) Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to have the thickness of the field plate oxide and the thickness of the gate oxide as claimed as a result of achieving a desired or required breakdown voltage and threshold voltage.

33. Regarding **claim 13**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode (17) is connected to the source region (21; Fig. 3, paragraph [0026])

34. Regarding **claim 14**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently (this is implied in the paragraph [0027], where Omura et al. disclose a voltage applied to each buried electrode 17, which obviously need a terminal connected to the buried electrode 17 to control the voltage).

35. Regarding **claim 15**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface

of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode(19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and wherein the drift region (12) has a graded doping concentration (see Fig. 15B) that increases from the part of the drift region (12) adjacent to the body region (13) to the part of the drift region (12) adjacent to the drain region (11; see Fig. 15B).

Omura et al. do not teach the gate-field plate insulator (18) being thicker than the field plate insulator (16), the doping concentration in the part of the drift region (12) adjacent to the drain region (11) being at least an order of magnitude greater than the doping concentration in the part of the drift region (12) adjacent to the body region (13).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the

breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

36. Regarding **claims 16-17**, Omura et al. teach the doping concentration (Fig. 15B), the drift region (12), the drain region (11), the body region (13).

Omura et al. do not teach, regarding to **claim 16**, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 50 times greater than the doping concentration in the part of the drift region adjacent to the body region, regarding to **claim 17**, the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region,

Parameters such as the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003], or the breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the doping concentration within the range as claimed in order to achieve desired device performance.

37. Regarding **claim 18**, Omura et al. teach further comprising a source contact (source electrode 21; Fig. 4, paragraph [0026]) and an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the

conductive material of the source electrode 21; Fig. 4, paragraph [0026]), the additional trench (the trench formed between the interlevel dielectric films 22) extending through the source region (14) to the body region (13), the conductive material in the additional trench (the conductive material of the source electrode 21 in the trench) connecting the source contact (21) to the source region (14) and to the body region (13).

38. Regarding **claim 19**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) at the first major surface (the top surface of 13), a body region (well layer 13; Fig. 2, paragraph [0023]) under the source region (14), a drift region (drift layer 12; Fig. 2, paragraph [0023]) under the body region (13), and a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) under the drift region (12), the drift region (12) having a doping concentration (see Fig. 15B) that increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11); and a plurality of insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) into the drift region (12), each of the insulated trenches (15) including at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) and separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) and separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate

insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]).

Omura et al. do not teach, the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13) and the gate-field plate insulator (18) being at least as thick as the field plate insulator (16).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

39. **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Onda et al. ("SIC Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol. 162, no. 1, 16 July 1997, pages 369-388).

Omura et al. teach, regarding to **claim 11**, the first conductivity type is n-type (the conductivity type of the source region; paragraph [0023]), the second conductivity type is p-type (the conductivity type of the body region; paragraph [0023]).

Omura et al. do not teach, regarding to **claim 2**, the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type (i.e. p-type), and regarding to **claim 11**, the conductive gate electrode is of p-type doped polysilicon.

In the same field of endeavor of semiconductor device, Onda et al. teach the conductive gate electrode is a p-type doped polysilicon (Fig. 1, page 371 line 27). Onda et al. also teach that p-type polysilicon is used to form an accumulation mode SiC trench MOSFET (page 371, lines 23-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Onda et al. and use the gate taught by Onda et al., because an accumulation mode SiC trench MOSFET can be formed as taught by Onda et al.

40. **Claims 3 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claims 1and 19 above, and further in view of Miyano et al. (JP 403211885A).

Regarding **claims 3 and 20**, Omura et al. teach the conductive gate electrode and the insulated trench.

Omura et al. do not teach, regarding to **claim 3**, the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning the gap between the side pieces, and regarding to **claim 20**, the conductive gate electrode in each of the insulated trenches includes two vertical side pieces spaced apart from each other and adjacent to the sidewalls on either side of the insulated trench, and a horizontal top piece spanning the gap between and connecting the two side pieces.

In the same field of endeavor of semiconductor device, Miyano et al. teach, regarding to **claim 3**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) has side pieces (the left side and the right pieces with deeper depth) spaced apart adjacent to the sidewalls on either side of the insulated trench (a trench; Fig. 1 and 2, [Application example]) and a top piece spanning the gap between the side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces), and regarding to **claim 20**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) in each of the insulated trenches (a trench; Fig. 1 and 2, [Application example]) includes two vertical side pieces (the left side and the right pieces with deeper depth) spaced apart from each other and adjacent to the sidewalls on either side of the insulated trench (a trench; see Fig. 1 and 2, [Application example]), and a horizontal top piece spanning the gap between and connecting the two side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces).

Miyano et al. also teach the shape of the gate reduces the capacitance between the gate and the drain, i.e. the bottom structure, and a high speed operation can be performed ([Operation]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Miyano et al. and use the gate taught by Miyano et al., because the speed of the device can be improved as taught by Miyano et al.

41. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 7 above, and further in view of Hshieh et al. (US 2001/0003367 A1).

Regarding **claim 8**, Omura et al. do not teach a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, the doping concentration in the doped contact region being higher than the doping in the rest of the body region.

In the same field of endeavor of vertical transistors, Hshieh et al. teach a doped contact region (P+ region 138; Fig. 2, paragraph [0025]) of the second conductivity type (p type) in the body region (in the P-body region; Fig. 2, paragraph [0025]) in contact with the conductive material (source metal layer 160; Fig. 2, paragraph [0025]) in the additional trench (source contact openings 150; Fig. 2, paragraph [0025]), the doping concentration in the doped contact region being higher than the doping in the rest of the body region (the doping concentration of P+ region is higher than P region). Hshieh et al. also teach the doped contact region 138 is used to reduce the parasitic resistance (paragraph [0025]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Hshieh et al. and use the doped contact region taught by Hshieh et al., because the parasitic resistance can be reduced as taught by Hshieh et al.

Response to Arguments

42. Applicant's amendments, filed 09/10/2009, overcome the objections to claims 11 and the rejections to claims 15-18 under 35 U.S.C. 112. The objections to claims 11 and the rejections to claims 15-18 under 35 U.S.C. 112 have been withdrawn.

43. Applicant's arguments filed 09/10/2009 have been fully considered but they are not persuasive.

44. On pages 7-9 of Applicant's Response, Applicant argues that the '455 reference fails to correspond to aspects of the claimed invention directed to the thickness of the gate-field plate insulator being greater than or equal to the thickness of the field plate insulator. The '455 reference teaches that the insulator between buried electrode 17 and gate electrode 19 (second insulating film 18) has a thickness between 400 to 450Å, whereas the insulator (first insulating film 16) for buried electrode 17 has a thickness of 3000 Å. Thus by expressly teaching that film 16 should be thicker than film 18, the '455 reference teaches away from the thickness of the gate-field plate insulator being greater than or equal to the thickness of the field plate insulator, as in the claimed invention.

45. The Examiner respectfully disagrees with Applicant's argument, because the '455 reference teaches that the thickness of the gate-field plate insulator 18 is determined by a threshold voltage and the thickness of the field plate insulator 16 is determined by a breakdown voltage, i.e. the thicknesses of these two layers depend on the application and for some applications (e.g. high threshold voltage and low breakdown voltage), the thickness of the gate-field plate insulator can be greater than or equal to the thickness of the filed plate insulator (paragraph [0031]). Although the '455 reference mentions 400 to 450Å and 3000 Å, they are given as examples (paragraph [0031]). The '455 reference also mentions the field plate insulator 16 is preferably thicker than the gate-field plate insulator 18, but '455 reference does not forbid using a device with the field plate insulator 16 thinner than the gate-field plate insulator 18 ([paragraph [0031]). Thus the '455 reference does not teach away from the invention.

46. On page 9 of Applicant's Response, Applicant argues that the cited portions of the '455 reference do not provide any indication regarding the actual level of impurity concentration in drift layer 12 near well layer 13 relative to the actual level of impurity concentration in drift layer 12 near substrate 11, let alone teach that the doping concentration in the drift region has a steeply graded concentration gradient as in the claimed invention. Accordingly, the rejections are improper and Applicant requests that they be withdrawn.

47. The Examiner respectfully disagrees with Applicant's argument, because the '455 reference teaches that the doping concentration has a graded concentration (Figs 16A to 16C) but does not teach the actual level. Finding the actual level is considered as a process of optimization and does not have a patentable weight.

48. On page 10 of Applicant's Response, Applicant argues that the Office Action, however, has not provided any evidence that replacing the '455 reference's gate electrode 19 with the '855 reference's gate electrode 3 would reduce the capacitance between the electrode and substrate 11 in the device of the '455 reference. As such, the Office Action's assertion that the combination would reduce the capacitance between gate 19 and substrate 11 are speculative at best.

49. The Examiner respectfully disagrees with Applicant's argument, because It would have been obvious to one of ordinary skill in the art at the time of invention was made to know that the '855 reference teaches the capacitance between the gate electrode 3 and the drain region 11 which corresponds to the capacitance between the gate electrode 19 and the buried electrode 17. Thus '855 reference teaches that the reduction in capacitance between the gate electrode 3 and the drain region 11 can improve the device speed, then the reduction in capacitance between the gate electrode 19 and the buried electrode 17 can also improve the speed. It is also well known

in the art of semiconductor manufacturing that reducing capacitance is the major factor in improving the speed of a MOSFET device.

50. On page 11 of Applicant's Response, Applicant argues that the Office Action improperly asserts that source electrode 21 extends in a trench through source layer 14 to well layer 13 in '455 reference. As is clearly shown in Figure 4, source layer 14 and well layer 13 each extend to the surface of the device where they connect to source electrode 21. As such, the source electrode 21 does not extend through source layer 14 to well layer 13 to connect the source electrode to the well layer, as does the additional trench filled with conductive material of the claimed invention. See, e.g., Applicant's Figure 3.

51. The Examiner respectfully disagrees with Applicant's argument, because source electrode 21 extends **horizontally** in a trench formed between interlevel dielectric films 22 through source layer 14 to well layer 13 to connect source electrode 21 to the well layer 13 as shown in Fig. 4 of '455 reference. Thus '455 reference still reads on this limitation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
1/30/2010